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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,446	09/30/2003	Belliappa Kuttanna	42P17025	7026

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Blakely Sokoloff Taylor & Zafman
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,446	KUTTANNA ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,18-21 and 23-30* is/are rejected.

7)☒ Claim(s) *17 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-30 are presented for examination. This office action is in response to the application filed on 9/30/2003.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 12/22/2003 is being considered by the examiner.

3. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. This **request** is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's

first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s), in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 10-13 and 28-30 are rejected under 35 U.S.C. 102(a) s being anticipated by Applicant's Admitted Prior Art (AAPA) pp204 and Figs. 1A-1C.

As to claim 10, AAPA discloses the invention as claimed. AAPA discloses a method, comprises detecting readiness of data (Page 3 lines 1-10 or block 3, checker and block 7, DRDY) one or more bus clocks(block 3) prior to data being ready to be transmitted to the processor (cache hit reads on this limitation since the requested data is provided to a processor from a fast access cache, in other words, during the cache hit cycle, requested data is provided to the processor is several bus clocks fasters than a normal memory access operation); and transmitting an early data ready indication (cache hit by a checker and block 7, DRDY) to a processor to drain a request seeking the data from a resource scheduler (block 6).

As to claim 11, AAPA discloses the invention as claimed in the above. AAPA further discloses transmitting a data ready indication to the processor when the data is ready; and filling a first level cache (FLC) of a data cache coupled with an execution unit (block 3, FLC).

As to claim 12, AAPA discloses the invention as claimed in the above. AAPA further discloses the detecting of the readiness of the data is performed by a memory controller (Block 3 , checker).

As to claim 13, AAPA discloses the invention as claimed in the above. AAPA further discloses wherein the transmitting of the early data ready indication is performed by the memory controller via a bus interface unit, the memory controller coupled with the bus interface unit via a front side bus (block 4 and Block 7).

As to claim 28, AAPA discloses the invention as claimed. AAPA discloses a machine-readable medium having stored thereon data representing sequences of instructions, the sequencing of instructions which, when executed by a machine, cause the machine to: detect readiness of data (Page 3 lines 1-10 or block 3, checker and block 7, DRDY) one or more bus clocks (block 3) prior to data being ready (cache hit reads on this limitation since the requested data is provided to a processor from a fast access cache, in other words, during the cache hit cycle, requested data is provided to the processor is several bus clocks fasters than a normal memory access operation) to be retrieved from memory (block 7 memory); and transmit an early data ready indication (cache hit by a checker and block 7, DRDY) to a processor (block 7, execution unit) to drain a request seeking the data from a resource scheduler (block 6).

As to claim 29, AAPA discloses the invention as claimed in the above. AAPA further discloses wherein the sequences of instructions which, when executed by the machine, further cause the machine to: transmit a data ready indication to the processor when the data is ready; and fill a data cache with the data, the data cache comprising a first level cache (FLC) (block 3, FLC) coupled with an execution unit.

As to claim 30, AAPA discloses the invention as claimed in the above. AAPA further discloses wherein the transmitting of the early data ready indication is performed by a memory controller (block 3 checker) via a bus interface unit (block 4 bus), the memory controller coupled with the bus interface unit via a front side bus (block 4 and block 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9, 14-16, 18, 19-21, and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Lehman et al. (Lehman) U.S. Patent No. 5,454,107 or Collins et al. (Collins) U.S. Patent No. 6,115,791..

As to claims 1 and 23, AAPA discloses a method, comprises accessing data cache for data in response to a request for the data (block 3), the request received from an instruction source; waiting for the data to be retrieved from memory if the data is not located in the data cache (block 3, checker); a data ready indication referring to the data being ready to be retrieved from the memory (block 7 DRDY) and a resource scheduler

(Block 7, RRQ), however, AAPA does not specifically discloses receiving an early data ready indication.

Lehman discloses an early data ready indication (ERDY col. 5 lines 26-33) for the purpose of decreasing the latency time thereby increasing the system access speed. Collins also discloses an early data ready indication (col. 9 lines 2-25, EPBRDY) for the purpose of decreasing the latency time thereby increasing the system access speed.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an early data ready indication of Lehman or Collins into the invention of AAPA for the advantages stated above.

As to claims 2 and 24, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses receiving the data ready indication; and filling the data cache with the data (block 3).

As to claims 3 and 25, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses inserting the request into the resource scheduler if the data is not located in the data cache (block 7 RRQ); and saving the request in the resource scheduler to wait for the data to be retrieved from the memory (block 7).

As to claims 4 and 26, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses accessing the data cache with the request while the data cache is being filled with the data (block 6 parallel processing); and meeting the request with the data from the data cache (Block 3).

As to claim 5, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses replaying the request to continue to snoop (Fig. 1 Refs. 124) the data cache for the data (block 6), the replaying comprising repeating the request through the data cache for a given number of times (Block 006, RRQ).

As to claim 6, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses at least one of an instruction and a load micro-operation ((block 6 line 4).

As to claim 7, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses the data cache is coupled with an execution unit, the data cache comprising a first level cache (FLC) and a second level cache (SLC) (blocks 3 and 4) .

As to claims 8 and 27, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses the resource scheduler is coupled with a bus interface (block 3) unit to receive the early data ready indication from a memory

controller (block 3, checker), the resource scheduler comprises a rescheduled request queue (RRQ) (blocks 6 and 7).

As to claim 9, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses wherein the memory controller is coupled with the bus interface unit via a front side bus (block 3).

As to claims 14 and 19, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses an apparatus, comprises a processor (block 2) having a resource scheduler (Block 6 RRQ) having one or more requests waiting for data to be loaded into a data cache including a first level cache (FLC) (block 3 FLC); and a memory controller (block 3 checker) coupled with the processor, the memory controller (block 5, checker) having an early data ready mechanism to detect readiness of the data one or more bus clocks prior to data being ready to be transmitted to the processor.

Lehman also discloses transmitting an early data ready indication scheduler (ERDY col. 5 lines 26-33) to the processor to drain the one or more requests from the resource. Collins also discloses an early data ready indication (col. 9 lines 2-25, EPBRDY) for the purpose of decreasing the latency time thereby increasing the system access speed.

As to claims 15 and 20, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses the processor further comprises a bus interface unit (block 3) to receive the transmitted early data ready indication from the memory controller and to transmit the early data ready indication to the resource scheduler having a rescheduled request queue (RRQ) (block 7).

As to claims 16 and 21, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses the bus interface unit is coupled with the memory controller via a front side bus (block 3).

As to claim 18, AAPA, Lehman, and Collins disclose the invention as claimed in the above. AAPA further discloses the data cache further comprises a second level cache (SLC) (block 6).

Allowable Subject Matter

6. Claims 17 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(571)-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner
December 26, 2005